BUGTRAP
INSTRUMENTATION

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BUGTRAP MODEL 8000
DYNAMIC RAM TESTER

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MODEL 8000 DYNAMIC RAM TESTER
THEORY OF OPERATION

SWITCH PANEL SELECTIONS

DEVICE: The device type must be selected, which "tells" the Model 8000 what size and configuration of DRAM is to be tested. For example, selecting "4164" (the most common part number for a 64K DRAM) sets up the DRAM tester for testing a 64K x 1 bit dynamic RAM, 4164 or equivalent. Making the device selection will also light a LED indicator at the bottom of the appropriate test socket to be used for the test.

ACCESS TIME: Next, the user must select the access time at which the DRAM will be tested. If the coding on the DRAM specifies a 150 nanosecond (ns) access time, the user would make the 150ns selection. The manufacturer specification for access time refers to the Row Address Strobe ($\overline{RAS}$) time and is generally used as the DRAM's operating speed rating. A 150 nanosecond selection sets up the Model 8000 to test the DRAM for minimum performance levels guaranteed by DRAM manufacturers for a 150ns DRAM. A good DRAM must pass the testing at its rated speed or faster.

One of the access time selections on the Model 8000 is labeled "REFRESH". The refresh specification of a DRAM refers to the maximum length of time a memory location can retain its data correctly before it needs to be accessed again, allowing for continued retention of the data. Without "refreshing" the memory, data would be lost.

The Model 8000 does a long-cycle test of the DRAM when "REFRESH" is selected. The maximum amount of time allowed by manufacturer specifications is inserted between each row address accessed to confirm that data is retained for a guaranteed minimum amount of time at each memory location. On some DRAMs, this means that each row address must be accessed every two milliseconds to retain data while other DRAMs require it every four or eight milliseconds. While a refresh type failure is very rare in an otherwise correctly performing DRAM, the selection is available to the user, even if infrequently used. The refresh test will take considerably longer than the other access time tests.

MODE: The only selection left to be made is for the mode of testing, "NORMAL" or "CONTINUOUS". In the normal mode, five complete test cycles are performed on the DRAM. Each test cycle consists of moving six different data patterns through all address locations of the DRAM, writing first and then reading. After all address locations (cells) have been written into, and read from, with all six data patterns five times each, the test will automatically stop. It may seem like this much testing would take a long time, but the entire test sequence on a 64K DRAM, for example, would take less than one second.

In the continuous mode, the testing would not automatically stop. It would continue as long as the DRAM kept performing correctly or until the user terminated the test. This continuous mode selection is especially helpful when an intermittent or thermal related failure of the DRAM is suspected. This mode can also be used to "burn-in" a DRAM before inserting it into your equipment. In either mode, normal or continuous, the test will automatically stop as soon as any DRAM failure occurs.

DRAM INITIALIZATION

When the "START TEST" switch is pushed, the DRAM being tested will be initialized. This consists of first powering up the DRAM with the proper voltages, in the proper order. After power-up, at least one millisecond is allowed before DRAM operation and RAS is held at a logic high (+5VDC) for at least 100 microseconds. The logic buffers to the test sockets are then turned on and a minimum of eight RAS cycles are executed before valid testing begins.

ADDRESSING

Each memory cell is accessed sequentially starting at the lowest order address location, address 0000..., and ending at the highest order location, address 1111..., and starting all over again at the lowest address location. An address location is determined by a combination of a row address and a separate column address, creating a type of matrix to select the proper memory cell, or cells.

These address locations are first written into with the appropriate data bit, a logic one or logic zero, depending on the data pattern in progress. After all locations have been written into, they are all read from while the Model 8000 verifies that the data being read is correct. After all locations have been read, the Model 8000 steps to a different data pattern and performs the cycle all over again, until all six data patterns have been used.

DATA PATTERNS

As mentioned, there are six different data patterns. One pattern consists of writing all logic "ones" to all address locations sequentially. Another has all logic "zeroes" written into the DRAM. The checkerboard pattern writes a logic "one" to one address location then a logic "zero" to the next, a logic "one" to the next, etc. The next pattern consists of inverting the checkerboard so that every location that received a "one" now gets a "zero" and vice-versa. Finally, two pseudorandom data patterns are generated.

RAS & CAS TIMING

Two major timing signals required for DRAM operation are the Row Address Strobe ($\overline{RAS}$) and the Column Address Strobe ($\overline{CAS}$). These two signals are responsible for locking in the necessary row address and column address locations. Both are needed to determine which memory cell is being used. In addition, the length of time $\overline{RAS}$ is at a logic low corresponds to the access time. If a DRAM is rated at 150ns, valid data must be available at the DRAM's output within the 150ns $\overline{RAS}$ signal, if in the read cycle. The Model 8000 verifies that the DRAM operation is correct within these strict timing parameters.

ERROR GENERATION

During testing, the Model 8000 verifies that all the DRAM inputs are operating correctly, that is, that none are either open or shorted. This includes the data input, $\overline{RAS}$, $\overline{CAS}$, R/$\overline{W}$ (read/write), and all address inputs.

Correct data output is also verified and is verified within the strict access time performance parameters already discussed. Multiple data patterns are used during testing to insure that all internal cells of the DRAM are operating correctly. This insures that no cells are stuck "high", stuck "low", or shorted to adjacent cells.

After the DRAM has gone through its initialization procedure and valid testing has begun, the "FAIL" indicator LED on the Model 8000 will light at the first occurrence of any DRAM failure. Testing will then automatically stop as further testing is pointless.

The "PASS" indicator LED will not light, however, until an entire "NORMAL" mode test sequence has been executed, whether in the normal or the continuous test mode. In the continuous mode, this "PASS" indicator will remain lit until a DRAM failure, if any, is encountered. If a DRAM failure is detected, the "PASS" LED will turn off, the "FAIL" LED will light and testing will automatically stop.

MODEL 8000 DYNAMIC RAM TESTER OPERATING INSTRUCTIONS

1. Turn on the power switch and check that the voltage indicator LEDs (+5VDC, +12VDC, −5VDC) are lit. Proceed if lit.

2. Select the type of DRAM device to be tested. If the part number on the DRAM looks unfamiliar, check for it in the cross reference chart.

3. Select the proper access time at which the DRAM is to be tested. There is no industry standard for the access time coding on the DRAM, so please check for the speed rating of the DRAM in the cross reference chart. It is not uncommon for a DRAM to pass at one speed faster than it is rated.

If "REFRESH" is selected, the test will take considerably longer than if any of the other access times are selected. The test cycle time is much slower to insure each address location retains its data for the guaranteed minimum amount of time necessary before being accessed.

4. Select either the "NORMAL" or "CONTINUOUS" test mode. In the normal mode, a single test sequence will be executed on the DRAM. This test sequence involves running six different data patterns, five times each, through all address locations of the DRAM.

In the continuous mode, testing of the DRAM doesn't stop unless a DRAM failure occurs or the user stops the test.

To stop the test while in the continuous mode, simply touch the "NORMAL" switch and watch for the "TEST IN PROGRESS" LED to turn off.

5. Now place the DRAM into the appropriate Z.I.F. (Zero-Insertion-Force) test socket. An LED was lit just below the appropriate socket when you selected the type of DRAM to be tested. Make sure that pin #1 of the DRAM is placed at the upper left corner of the test socket, closest to the locking handle. Now, push down the locking handle to lock the DRAM in place and assure good electrical contact. Be sure to only have one DRAM in the bank of test sockets at any one time.

CAUTION! Only place a 4116 or equivalent DRAM in the left-most test socket. +12VDC and −5VDC are present at this socket and will damage other types of DRAMS.

6. Push the "START TEST" switch and monitor for the "PASS" or "FAIL" test results. The "FAIL" indicator will light at the first DRAM failure encountered, but the "PASS" indicator will not light until an entire "NORMAL" test sequence has been completed. If the user has selected the "CONTINUOUS" mode, the "PASS" indicator will extinguish and the "FAIL" indicator will light if any DRAM failure occurs during the extended testing. The testing will automatically stop at the first failure indication.

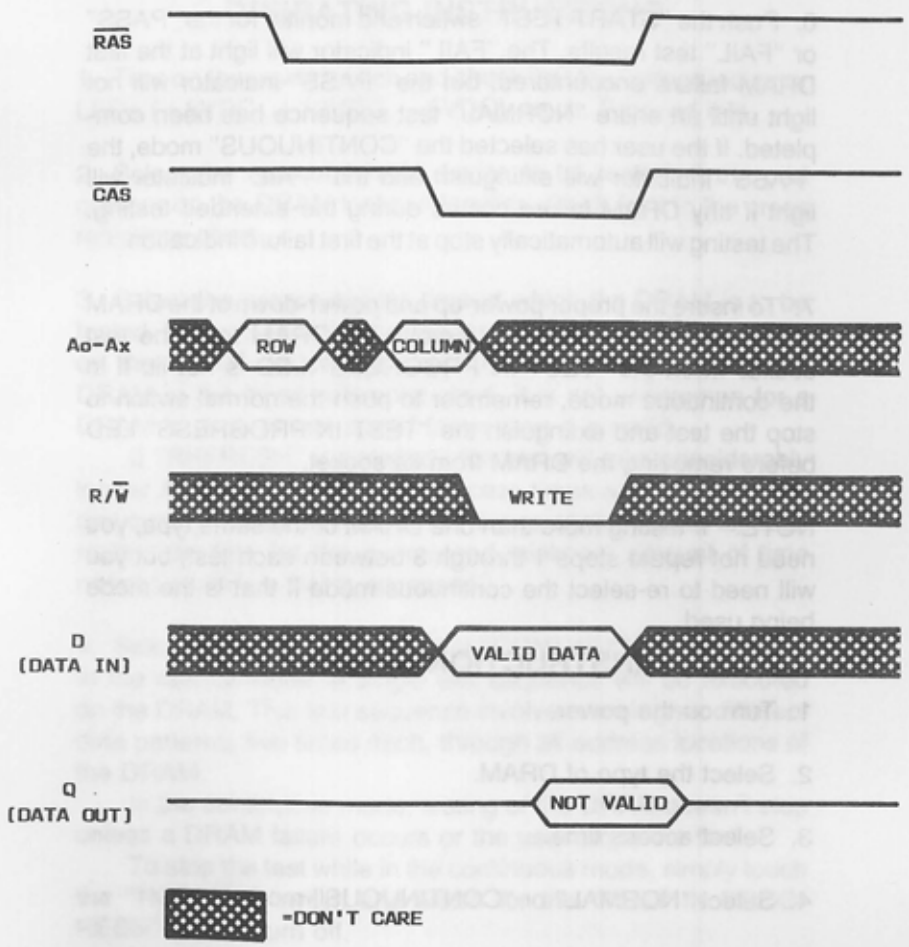
7. To insure the proper power-up and power-down of the DRAM being tested, only insert or remove the DRAM from the test socket when the "TEST IN PROGRESS" LED is not lit. If in the continuous mode, remember to push the normal switch to stop the test and extinguish the "TEST IN PROGRESS" LED before removing the DRAM from its socket.

NOTE: If testing more than one DRAM of the same type, you need not repeat steps 1 through 3 between each test, but you will need to re-select the continuous mode if that is the mode being used.

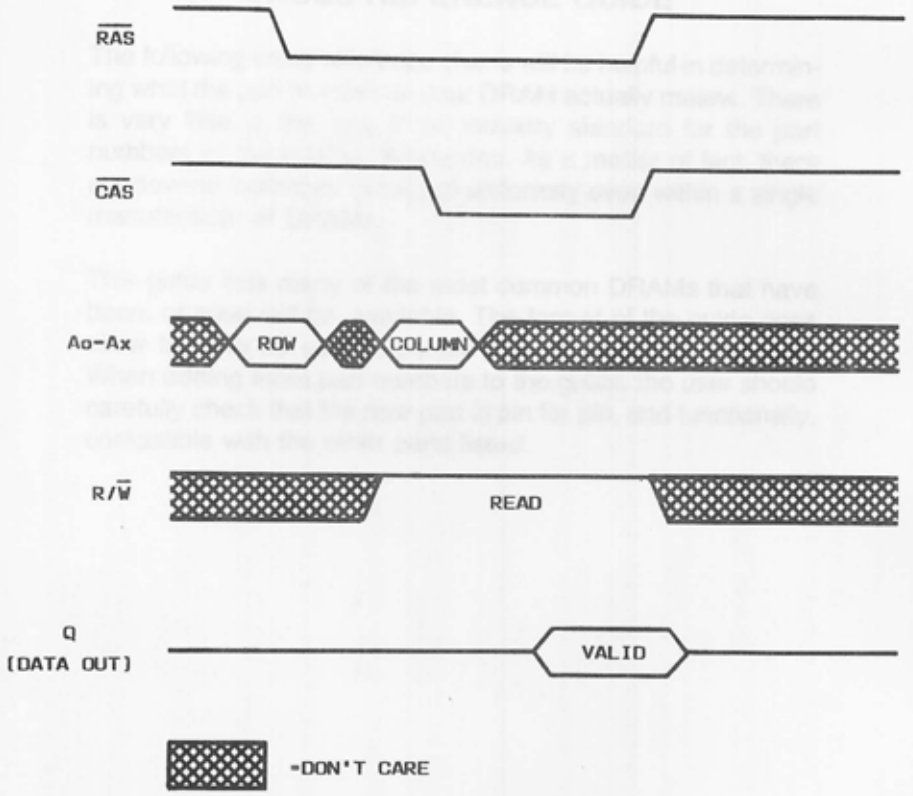
INSTRUCTION SUMMARY

1. Turn on the power.
2. Select the type of DRAM.
3. Select access time.
4. Select "NORMAL" or "CONTINUOUS" mode.
5. Lock DRAM into indicated Z.I.F. test socket.
6. Push the start switch and monitor test results.
7. Remove DRAM from it's socket once the "TEST IN PROGRESS" LED turns off. If in the continuous mode, push "NORMAL" to stop the test and extinguish the "TEST IN PROGRESS" LED.

WRITE CYCLE TIMING



READ CYCLE TIMING



CROSS REFERENCE GUIDE

The following cross reference charts will be helpful in determining what the part number on your DRAM actually means. There is very little in the way of an industry standard for the part numbers or the access time codes. As a matter of fact, there are several instances of lack of uniformity even within a single manufacturer of DRAMs.

This guide lists many of the most common DRAMs that have been, or soon will be, available. The format of the guide does allow for it to be easily updated and expanded by the user. When adding more part numbers to the guide, the user should carefully check that the new part is pin for pin, and functionally, compatible with the other parts listed.

DRAM SIZE: 16k (+12,+5,-5VDC only)
COMMON DESIGNATION: 4116

MANUFACTURER	ACCESS TIME					
	100ns	120ns	150ns	200ns	250ns	300ns
AMD			AM9016F	AM9016E	AM9016D	AM9016C
AT & T						
FAIRCHILD			F16K-2	F16K-3 F4116-3	F16K-4 F4116-4	
FUJITSU			MB8116H	MB8116E	MB8116N	
HITACHI			HM4716A-2	HM4716-3	HM4716-4	
HYUNDAI						
INMOS						
INTEL			P2117-2	P2117-3	P2117-4	
ITT			ITT4116-2	ITT4116-3	ITT4116-4	
MICRONTECH						
MITSUBISHI			M5K4116P-2	M5K4116P-3		
MOSTEK			MK4116-2	MK4116-3/-83/-93	MK4116-4/-84/-94	
MOTOROLA			MCM4116B-15	MCM4116B-20	MCM4116B-25	MCM4116B-30
NATIONAL		MM5290-1	MM5290-2	MM5290-3	MM5290-4	
NEC		uPD416-5	uPD416-3	uPD416-2	uPD416-1	uPD416
OKI				MSM3716-3		
PANASONIC						
SAMSUNG						
SGS			M4116			
SIEMENS			HYB4116-P2	HYB4116-3/-P3	HYB4116-4	
SIGNETICS			2690-2	2690-3	2690-4	
T.I.			TMS4116-15	TMS4116-20	TMS4116-25	
TOSHIBA			TMM416-2	TMM416-3	TMM416-4	
TRISTAR						

DRAM SIZE: 16k (+5 only)

COMMON DESIGNATION: 2118

MANUFACTURER	ACCESS TIME					
	100ns	120ns	150ns	200ns	250ns	300ns
AMD						
AT & T						
FAIRCHILD						
FUJITSU	MB8117,8118-10	MB8117,8118-12				
HITACHI	HM8416A-3	HM8416A-4				
HYUNDAI						
INMOS						
INTEL		2118-4	2118-7			
ITT						
MICRONTECH						
MITSUBISHI						
MOSTEK	MK4516-10	MK4516-12	MK4516-15		MKB4516-80	MKB4516-81
MOTOROLA	MCM4517-10	MCM4517-12 MCM6665C-12	MCM4517-15 MCM6665C-15	MCM4517-20		
NATIONAL						
NEC	uPD2118-3					
OKI						
PANASONIC						
SAMSUNG						
SGS						
SIEMENS						
SIGNETICS						
T.I.						
TOSHIBA						
TRISTAR						

DRAM SIZE: 64k

COMMON DESIGNATION: 4164

MANUFACTURER	ACCESS TIME					
	100ns	120ns	150ns	200ns	250ns	300ns
AMD	AM9064-10	AM9064-12	AM9064-15			
AT & T						
FAIRCHILD		F64K-12	F64K-15	F64K-20 F4164-20		
FUJITSU	MB8264,65,66A-10	MB8264,65,66A-12	MB8264,65,66A-15	MB8264,65-20		
HITACHI		HM4864-1 HM4864A,65A-12	HM4864-2 HM4864A,65A-15	HM4864-3 HM5864A,65A-20		
HYUNDAI						
INMOS	IMS2600-10	IMS2600-12	IMS2600-15			
INTEL			2164A-15	2164A-20		
ITT						
MICRONTECH		MT4264-12	MT4264-15	MT4254-20		
MITSUBISHI		M5K4164-12	M5K4164-15	M5K4164-20		
MOSTEK	MK45H64-10	MK45H64-12/-81	MK4564-15/-82/-92	MK4564-20/-83	MK4564-25/-84	
MOTOROLA		MCM6665B-12	MCM6665A-15/B-15	MCM6665A-20/B-20		
NATIONAL		NMC4164-12	NMC4164-15	NMC4164-20		
NEC	uPD4164-2	uPD4164-12	uPD4164-15/-3	uPD4164-0/-20	uPD4164-1	
OKI		MSM3764-12	MSM3764-15	MSM3764-20		
PANASONIC			MN4164-15	MN4164-20		
SAMSUNG						
SGS						
SIEMENS			HYB4164-2	HYB4164-3		
SIGNETICS						
T.I.		TMS4164-12	TMS4164-15	TMS4164-20	TMS4164-25	
TOSHIBA		TMM4164-2	TMM4164-3	TMM4164-4		
TRISTAR		KM4164A-12	KM4164A-15	KM4164A-20		

DRAM SIZE: 128K (PIGGYBACK)

COMMON DESIGNATION: 41128

MANUFACTURER	ACCESS TIME					
	100ns	120ns	150ns	200ns	250ns	300ns
AMD						
AT & T						
FAIRCHILD						
FUJITSU						
HITACHI				HM48128P-2		
HYUNDAI						
INMOS						
INTEL						
ITT						
MICRONTECH						
MITSUBISHI						
MOSTEK			MK4128-15	MK4128-20	MK4128-25	
MOTOROLA				MCM66128L20		
NATIONAL						
NEC						
OKI						
PANASONIC						
SAMSUNG						
SGS						
SIEMENS						
SIGNETICS						
T.I.			TMS41128-15	TMS41128-20		
TOSHIBA						
TRISTAR						

DRAM SIZE: 256k

COMMON DESIGNATION: 41256

MANUFACTURER	ACCESS TIME					
	100ns	120ns	150ns	200ns	250ns	300ns
AMD						
AT & T						
FAIRCHILD						
FUJITSU	MB81256,257-10	MB81256,257-12	MB81256,257-15	MB81256,257-20		
HITACHI		HM50256,257-12	HM50256,257-15	HM50256,257-20		
HYUNDAI						
INMOS						
INTEL						
ITT						
MICRONTECH		MT1256-12	MT1256-15	MT1256-20		
MITSUBISHI		M5M4256,257-12	M5M4256,257-15	M5M4256,257-20		
MOSTEK		MK4556-12	MK4556-15	MK4556-20		
MOTOROLA	MCM6256-10	MCM6256-12	MCM6256-15	MCM6256-20		
NATIONAL						
NEC		uPD41256,257-12	uPD41256,257-15	uPD41256,257-20		
OKI	MSM41256-10	MSM41256-12 MSM37256-12	MSM41256-15 MSM37256-15	MSM37256-20		
PANASONIC						
SAMSUNG						
SGS						
SIEMENS						
SIGNETICS						
T.I.	TMS4256,257-10	TMS4256,257-12	TMS4256,257-15	TMS4256,257-20		
TOSHIBA		TMM41256-12	TMM41256-15	TMM41256-20		
TRISTAR						

DRAM SIZE: 1 Megabit

COMMON DESIGNATION: 411000

MANUFACTURER	ACCESS TIME					
	100ns	120ns	150ns	200ns	250ns	300ns
AMD						
AT & T			M411024-15			
FAIRCHILD						
FUJITSU			MB811000-15			
HITACHI						
HYUNDAI						
INMOS						
INTEL						
ITT						
MICRONTECH						
MITSUBISHI						
MOSTEK						
MOTOROLA						
NATIONAL						
NEC			D411000D,01D			
OKI						
PANASONIC						
SAMSUNG						
SGS						
SIEMENS						
SIGNETICS						
T.I.						
TOSHIBA	TMM411000,01-10		TMM411000,01-12			
	TC511000,01-10		TC511000,01-12			
TRISTAR						

DRAM SIZE: 16k x 4 bit

COMMON DESIGNATION: 4416

MANUFACTURER	ACCESS TIME					
	100ns	120ns	150ns	200ns	250ns	300ns
AMD						
AT & T						
FAIRCHILD						
FUJITSU	MB81416-10	MB81416-12	MB81416-15			
HITACHI		HM48416A-12	HM48416A-15	HM48416A-20		
HYUNDAI						
INMOS						
INTEL						
ITT						
MICRONTECH						
MITSUBISHI		M5M4416-12	M5M4416-15			
MOSTEK						
MOTOROLA						
NATIONAL						
NEC						
OKI						
PANASONIC						
SAMSUNG						
SGS						
SIEMENS						
SIGNETICS						
T.I.		TMS4416-12	TMS4416-15	TMS4416-20	TMS4416-25	
TOSHIBA						
TRISTAR						

DRAM SIZE: 64k x 4 bit
COMMON DESIGNATION: 4464

MANUFACTURER	ACCESS TIME					
	100ns	120ns	150ns	200ns	250ns	300ns
AMD						
AT & T						
FAIRCHILD						
FUJITSU			MB81464			
HITACHI		HM50464,465-12	HM40464,465-15	HM50464,465-20		
HYUNDAI						
INMOS						
INTEL						
ITT						
MICRONTECH		MT4064-12	MT4064-15	MT4064-20		
MITSUBISHI		M5M4464P-12	M5M4464P-15			
MOSTEK						
MOTOROLA						
NATIONAL						
NEC			uPD41254-15	uPD41254-20		
OKI						
PANASONIC						
SAMSUNG						
SGS						
SIEMENS						
SIGNETICS						
T.I.	TMS4464-10	TMS4464-12	TMS4464-15	TMS4464-20		
TOSHIBA			TMM41464P-15			
TRISTAR						

DRAM SIZE: 256k x 4 bit

COMMON DESIGNATION: 44256

MANUFACTURER	ACCESS TIME					
	100ns	120ns	150ns	200ns	250ns	300ns
AMD						
AT & T			M441024-15			
FAIRCHILD						
FUJITSU						
HITACHI						
HYUNDAI						
INMOS						
INTEL						
ITT						
MICRONTECH						
MITSUBISHI						
MOSTEK						
MOTOROLA						
NATIONAL						
NEC						
OKI						
PANASONIC						
SAMSUNG						
SGS						
SIEMENS						
SIGNETICS						
T.I.						
TOSHIBA						
TRISTAR						

SPECIFICATIONS *

DRAM TYPES:
16K(+5, +12, −5VDC), 16K(+5VDC),
128K(piggyback), 256K, 1 Megabit, 16K x 4,
64K x 4, 256K x 4

ACCESS TIME SELECTIONS:
100ns, 120ns, 150ns, 200ns, 250ns, 300ns
REFRESH (long cycle)

DATA PATTERNS:
All logic ones
All logic zeroes
Checkerboard
Inverted Checkerboard
Pseudorandom
Inverted pseudorandom

MODES:
Normal: Tests DRAMs with all data patterns, five times each.
Continuous: Allows for extended testing of DRAM.

ERROR DETECTION:
Single bit data errors
Open and shorted inputs
Timing and speed related errors
Memory retention (REFRESH)

OPERATING TEMPERATURE:
+32° to +100°F

TEST TIMES:
Test times will vary depending on the size of DRAM being tested and the access time at which it is being tested. Typical test times with "150ns" or "REFRESH" selected are:

	150ns	REFRESH
16K	0.2 seconds	5 seconds
64K	0.8 seconds	21 seconds
128K	1.5 seconds	21 seconds
256K	3.0 seconds	42 seconds
1 Meg	12.0 seconds	2.75 minutes
16K x 4	0.2 seconds	5 seconds
64K x 4	0.8 seconds	21 seconds
256K x 4	3.0 seconds	42 seconds

POWER:
Input voltage - 95 VAC to 130 VAC or
190 VAC to 260 VAC
Input frequency - 47 Hz to 450 Hz

DIMENSIONS:
8.68 in. x 2.79 in. x 17.08 in.
(220.47 mm. x 70.87 mm. x 433.83 mm.)

WEIGHT:
3 lbs., 12 oz.
(1.7 kg.)

* Subject to change without notice.